Dr. Durgesh Nandan
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Career Summary

A result-oriented leader with more than 7 years of teaching experience and 1-year industry experience with effective communicator, exceptional presentation skills & abilities in leading cross-cultural teams & establishing relationship.

Previously working as a role of **faculty under SMDP-C2SD project at ECE Department in National Institutes of Technology, Patna (Bihar)**.

Currently working as a role of **Research Mentor in Accendere Knowledge Management Services Pvt. Ltd. (100% subsidiary of CL Educate Ltd.) and Adjunct Professor at Aditya Engineering College, Surampalem (A.P)**

Education

Examination	School /college / Board / University	Duration	Percentage /CGPA
PhD	Jaypee University of Engineering & Technology, Guna	2014- 2018 (08-10-2018)	8 (Course Work)
PGDIPR	IGNOU	2018	Ongoing
M.TECH (MEVD)	Technocrats Institutes of Technology, Bhopal (R.G.P.V)	2010 - 2013	79.4 % (First with Distinction.)
B.E.(EC)	Bansal College of Engineering, Mandideep (R.G.P.V.)	2005 - 2009	70.34% (First)
High Secondary (10+2)	A.N.D.C, Shahpur Patory (Bihar Board)	2001	76.3% (First with Distinction.)
High School (10^{th})	G.B.H.S, Shahpur Patory (Bihar Board)	1999	61.2% (First)

Employment Details

Research:

- Currently worked as a role of the **Research Mentor in Accendere Knowledge Management Services Pvt. Ltd. (100% subsidiary of CL Educate ltd.) and Adjunct Professor at Aditya Engineering College, Surampalem (A.P)** from 21th September 2018 to till date.
- Worked as a full-time research scholar on the research topic of "**Design and analysis of an efficient architecture of logarithmic multiplier and its applications"** in **Jaypee University**

of Engineering and Technology, Guna (MP) from 07th August 2014 to 21 April 2018. For PhD thesis refer to http://hdl.handle.net/10603/218727.

Teaching:

- Worked as a **faculty under SMDP-C2SD project at ECE Department in National Institutes of Technology, Patna (Bihar)** from 25th April 2018 to 20th September 2018.
- Worked as an **Asst. professor** in IASSCOM fortune institutes of technology, Bhopal (M.P) from 5th April 2013 to 31st July 2014.

Other work:

- Worked as a **Head of department** (E.C) in IASSCOM fortune institutes of technology, Bhopal (M.P) from 5th April 2013 to 31st July 2014.
- Worked as an **Asst. Exam controller** in IASSCOM fortune institutes of technology**,** Bhopal (M.P) From December 2013 to June 2014.
- Worked as Quantitative aptitude trainer in Engineering College for preparing campus interview.

Area of Research Interest

- Artificial intelligence/Machine Learning for Digital Signal Processing
- Neural Network Circuits by using Logarithm Number System
- VLSI Systems Design for Signal Processing Algorithms
- VLSI Systems Design for Speech Processing Algorithms
- Hardware architecture for Image Denoising
- Hardwar security and Cryptography
- Reversible Logic for Signal Processing & Quantum computing
- Computer arithmetic Circuits and Logarithm Number System

Area of Subject Interest

- Basic of electronics
- Digital signal processing
- Electronic devices
- Computer arithmetic
- CMOS and ASIC VLSI design
- Digital electronics

Research Publication

Journal Paper:

1. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, **"An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition,"** Elsevier, VLSI the integration journal, Vol. 58, pp. 134-141, June 2017, DOI: 10.1016/j.vlsi.2017.02.003 (**SCI**).
2. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"An errorless Gaussian filter for image processing by using expanded operand decomposition logarithm multiplication,"** Springer, Journal of ambient intelligence and humanized computing**,** DOI:10.1007/s12652-018-0933-x, 2018 **(SCI,** In Press**).**
3. Mahesh Kumar, **Durgesh Nandan** and Sanjeev Kumar, "**Statistical Analysis of Lower and Raised Pitch Voice Signal and its Efficiency Calculation**," Traitement du Signal, 2019 (SCI, In Press).

4. Prashant Srivastava, Yogesh Srivastava, Bhagat Singh, Arun kumar Pandey and **Durgesh Nandan**, "**Investigation of Optimal Process Parameters for Laser Cutting of Inconel-718 Sheet**," Part C: Journal of Mechanical Engineering Science, 2019 (**SCI**, In Press).
5. Sanjeev Kumar, **Durgesh Nandan**, Amit Shivhare and Ravi Kumar "**A Multiple L-Shaped Slot Loaded Antenna with Multiband Circularly Polarized for WLAN and WiMAX Applications,"** International Journal of Engineering and Advanced Technology (IJEAT), Volume-8 Issue-6S, pp. 965-969, August 2019 **(Scopus).**
6. E. Jagadeeswara Rao, **Durgesh Nandan**, R.V. Vijaya Krishna and K. Jayaram Kumar, "**A Systematic Review of Multipliers: Accuracy and Performance Analysis,"** International Journal of Engineering and Advanced Technology (IJEAT), Volume-8 Issue-6S, pp. 965-969, August 2019 **(Scopus).**
7. D.S.V. Suma Priya, D. Esther Rani, A. Pavan Shankar Sai, A. Konda Babu, **Durgesh Nandan**, "**Review on importance of Machine Learning and Artificial Intelligence in real life problem solving**" Journal of Computational and Theoretical Nanoscience, 2019 **(Scopus).**
8. R. Rohini, N. V. Satya Narayana and **Durgesh Nandan** "**A crystal view on design of FIR filter**" Journal of Computational and Theoretical Nanoscience, 2019 **(Scopus).**
9. G. Devananda Kumar, Vidheya Raju and **Durgesh Nandan** "**A review on smart irrigation system**" Journal of Computational and Theoretical Nanoscience, 2019 **(Scopus).**
10. Padala Neeraja and **Durgesh Nandan** "**Smart home by using IOT system: A succinct study**" Journal of Computational and Theoretical Nanoscience, 2019 **(Scopus).**
11. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"An efficient VLSI architecture design of Leading One Detector,"** International journal of pure and applied mathematics, Vol.118 (14), pp. 267-272, 2018 (**Scopus**).
12. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"65 years journey of logarithm multiplier,"** International journal of pure and applied mathematics, Vol.118 (14), pp. 261-266, 2018 (**Scopus**).
13. **Durgesh Nandan**, Mahajan, A. and Kanungo, J. (2018), **"An efficient architecture of Iterative Logarithmic Multiplier,"** *International journal of engineering & technology (UAE).* Vol.7 (2.16), pp. 24-28, 2018 (**Scopus**).
14. **Durgesh Nandan**, Anurag Mahajan and Jitendra Kanungo**, "Implementation of Leading One Detector based on reversible logic for logarithmic arithmetic,"** International Journal of Computer Applications, Vol.173 (8), pp. 40-45, Sep. 2017.
15. Parvin Akhter, Sachin Bandewar, **Durgesh Nandan, "Logarithmic Multiplier: An Analytical Review**" International Journal of Engineering Research, Vol.5 (8), pp: 721-723, August 2016.

International Conference paper:

16. Kaushal Kumar, **Durgesh Nandan** and Ritesh Kumar Mishra, "**The hardware design prospective of object detection by using background subtraction techniques: an analytical review,**" SoCTA 2018, NIT Jalandhar (**Scopus**).
17. **Durgesh Nandan**, Anurag Mahajan and Jitendra Kanungo, "**An Efficient antilogarithmic converter by using 11-regions error correction scheme,**" IEEE 4th International Conference on Signal Processing, Computing and Control (ISPCC 2017), JUIT, Waknaghat, pp. 118-121, 21-23 Sep.2017 (**Scopus**).
18. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An efficient VLSI architecture for Iterative Logarithmic Multiplier,**" IEEE 4th International conference on signal processing and integrated networks (SPIN), Noida, pp.419-423, Feb.2017 (**Scopus**).
19. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An Efficient VLSI architecture design for antilogarithmic converter by using the error correction scheme**," IET

International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016, DOI: 10.1049/cp.2016.1445.

20. Sachet Jamliya, Anurag Mahajan, Abhishek Choubey and **Durgesh Nandan**, "**An efficient VLSI architecture of multiplier-less 1-D DWT using CSD technique**," IET International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016.
21. Khushboo Patel, Vibha Tiwari, and **Durgesh Nandan**, **"Crosstalk mitigation of network on chip: an analytical review"** IEEE International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, pp. 378-383, 3-5 March 2016, DOI: 10.1109/ICEEOT.2016.7755393 (**Scopus**).
22. **Durgesh Nandan** and Shivendra Singh, **"The comparative result of symmetric encryption techniques,"** Springer indexed ICICIC Global, Chennai, Dec. 2012.
23. **Durgesh Nandan** and Shivendra Singh, **"Key Reconfiguration Scheme for DES Algorithm,"** Springer indexed ICICIC Global, Chennai, Dec. 2012.
24. S. Manasa, P. Hemanth, P. Bala Srinivas and **Durgesh Nandan**, **"A Literature Review on Prevention of Accident by Using IoT,"** Springer indexed ICMETE-2019 / "Lecture Notes in Networks and Systems", SRMIST Ghaziabad, 28-27 Sep. 2019 (**Scopus**).
25. E. Sai Sravani, A.V. Sreehitha, A. Konda Babu, and **Durgesh Nandan**, **"Evaluation and Study of IoT Entrances,"** Springer indexed ICMETE-2019 / "Lecture Notes in Networks and Systems", SRMIST Ghaziabad, 28-27 Sep. 2019 (**Scopus**).
26. R. Vasantha Lakshmi, S. Shyam Mohana, N. Radha, and **Durgesh Nandan**, **"Periodical Development of Digital Watermarking Technique,"** Springer indexed ICMETE-2019 / "Lecture Notes in Networks and Systems", SRMIST Ghaziabad, 28-27 Sep. 2019 (**Scopus**).
27. K. Sowmya, P. Bujji Babu, **Durgesh Nandan**, "**Survey on the impact of FSM design for high-performance architecture evaluation,**" Springer indexed ICMETE-2019 / "Lecture Notes in Networks and Systems", SRMIST Ghaziabad, 28-27 Sep. 2019(**Scopus**).
28. Vanaja Kandubothula, Rajyalakshmi Uppada, **Durgesh Nandan**, "**A review on detection of breast cancer cells using various techniques,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
29. Y. Sasi Supritha Devi, T. Kesava Durga Prasad, Krishna Saladi, **Durgesh Nandan**, "**Analysis of precision agriculture technique by using machine learning and IOT,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
30. P. Sai Ramya, **Durgesh Nandan**, "**Analysis of Security issues and possible solutions in the Internet of Things for home automation system,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
31. P. Sai Ramya, **Durgesh Nandan**, "**Analysis of Security issues and possible solutions in the Internet of Things for home automation system,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
32. P. Mani Sai Jyothi, **Durgesh Nandan**, "**Utilization of the internet of things in agriculture possibilities and challenges,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
33. A. Krishna Chaitanya, Ch. Kartheek, **Durgesh Nandan**, "**Real-time Face Recognition and Tracking for Criminal Revealing,**" Springer indexed 4th International conference on Soft Computing: Theories and Applications (SOCTA-2019) / Advances in Intelligent Systems and Computing (AISC), NIT Patna (**Scopus**).
34. **Durgesh Nandan**, Kaushal Kumar, Jitendra Kanungo, Ritesh Kumar Mishra**, "Compact and Errorless 16-Region Error Correction Scheme for Antilogarithm Converter," 6th** IEEE

Uttar Pradesh Section International Conference on Electrical and Computer Engineering (UPCON-2019), 09-10 Nov. 2019, AMU Aligarh (Scopus).

Book Publication (Author/Editor)

1. **Durgesh Nandan** and Shivendra Singh, **"Key Reconfiguration Scheme for DES Algorithm,"** Lambert academic publishing, Germany, ISBN: 978-3-659-89769-6.
2. **Durgesh Nandan**, Basant Kumar Mohanty, Sanjeev Kumar and Rajeev Kumar Arya, **"VLSI Architecture for Signal, Speech and Image Processing,"** Apple Academic Press, USA, In Press.
3. **Durgesh Nandan**, Sangeeta Singh, Rajeev Kumar Arya and Millie Pant, **"Nature-Inspired Algorithms in Soft Computing Architecture and Applications for Real-World Problems,"** Apple Academic Press, USA, In Press.

Invited Lectures and Talks

1. Delivered Two days Talks on "Recent trends in Digital VLSI Design" at Vidyavardhaka College of Engineering, Mysore from 08-09 February 2019.
2. Delivered one day Talk on "Speech Processing: An overview and real time applications possibilities" in one-week FDP on Recent Research trends in Signal Processing at Aditya Engineering College, Surampalem on 27th April 2019.
3. Delivered Two-week Talk and Hands on research article writing tools on "Research Methodology & Outcomes" at Aditya Engineering College, Surampalem from 30th April 2019 to 10th May 2019.
4. Delivered one day Talk on "Arithmetic circuits with logarithmic number system" in one-week FDP on Recent Research trends in Digital VLSI Design at Aditya College of Engineering and Technology, Surampalem on 30th May 2019.

FDP/Workshop Organized

1. Organized one-week FDP on "Recent Research trends in Signal Processing" at Aditya Engineering College, Surampalem as coordinator from 23th April 2019 to 27th April 2019.
2. Organized Two-week Workshop on "Research Methodology & Outcomes" at Aditya Engineering College, Surampalem as a Convenor from 30th April 2019 to 10th May 2019.
3. Organized one-week FDP on "Recent Research trends in Digital VLSI Design" at Aditya College of Engineering and Technology, Surampalem as coordinator from 27th May 2019 to 31th May 2019.

Professional Trainings Attended

- Attended in the AI/ML workshop held at Engineering Staff College of India, Hyderabad on March 3, 2019.
- Attended a one-week GIAN course on "Logic design under paradigm of rebooting computing" from 25-29 Dec.2017 at IIT Roorkee.
- Attended a one-week course on "Hands on session on VLSI design tools" from 18 -22 Dec. 2017 at NIT Delhi.
- Attended UGC funded a one-week workshop on "VLSI design & sensors in systems" from March 20-25, 2017 at School of physics, University of Hyderabad, Hyderabad.
- Attended a two days National workshop on "MATLAB application in science & engineering" from February 11-12, 2017 at JUET, Guna.

- Attended a two-week GIAN course on "VLSI Architectures for Signal Processing and machine learning" from 19-30 December 2016 at IIT Kharagpur.
- Attended in National workshop on "High-performance VLSI Architectures for Digital Signal Processing Applications: Design and Implementations" from 9-11 September 2016 at JUET, Guna (MP).
- Attended in faculty recharge program on "VLSI Design" from 14-16 July 2015 at JUET, Guna (MP).
- Attended a two days National workshop on "Low Voltage and Low Power VLSI Design" from 22-23 August 2014 at JIIT, Noida.
- Attended a two- week ISTE workshop on "SIGNAL & SYSTEM" under the national mission on education through ICT which is organized by IIT, Kharagpur from 02-12 January 2012.
- Attended a two- week ISTE workshop on "ANALOG ELECTRONICS" under the national mission on education through ICT which is organized by IIT, Kharagpur.

Academic advising

- **PhD – 01 (In Progress).**
- M. Tech Dissertation – 01

Research Mentor activities

Reviewer of SCI Journal:

- Journal of Circuits, Systems and Computers, World Scientific.
- Circuit, systems and signal processing, Springer
- IEEE Access
- Biomedical research, Allied Academies Journals.

Reviewer of Scopus Journal:

- International journal of engineering and technology innovation.
- The Institution of Engineers (India) Series B.
- Halliyan
- Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
- Recent Advances in Electrical & Electronic Engineering

Reviewer of International conference: (1) ICSPT'2013, (2) ICMASCTS'2014, (3) ICSIN'2014, (4) ICSPIE'2014, (5) ICTMASCS'2014, (6) ICSPCT 2014, (7) IJ--IS, (8) WSCNIS'2015, (9) WCI-2015, (10) ADMMET'2015, (11) ICCTIS'2015, (12) GAMEPEC 2015, (13) ICCEA'2015, (14) ISySM'2015, (15) PIAMSE'2015, (16) ICED 2016, (17) AVAREIT'2016, (18) AREITIC'2016, (19) ARECAS'2016, (20) ARONCAS'2016, (21) APPEMSE'2016, (22) AR2BIO-ICEMIT-RAIEIC'2016, (23) ICCCSIT-2016, (24) ICCITR'2016, (25) WCCAIS'16, (26) COMSIT'2016, (27) ENVICET'2016, (28) SCIEMATHIC'2016, (29) SYMINTECH'2016, (30) PROCSIT'2016, (31) WICOIS'2016, (32) I2BM'2017, (33) APPEMSE'2017, (34) ICACCI-2017, (35) ICOBSS'2017, (36) ICOCOE'2017, (37) SYMINTECH'2017, (38) CICN 2016, (39) ICCDMTA 2017, (40) PIAMSE'2017, (41) RENCES'2017, (42) I4CT'2015, (43) I4CT'2016, (44) SIRS-2015, (45) SIRS-2017, (46) SIRS-2018, (47) WCITCA'2015, (48) WCITCA'2016, (49) ISTA-2018, (50) I2CT 2019, (51) ICICRS 2019, (52) ICIIP 2019, (53) IEMECON 2019

TPC Member: (1) ICITA'2014, (2) GSCIT' 2015, (3) ENCINS' 2015, (4) ICCAAD' 2015, (5) ICCVIA' 2015, (6) IBMSGS' 2015, (7) GSCIT 2016, (8) ISTA-2017, (9) WSMEAP' 2015, (10) WSMEAP 2016, (11) WSCAR' 2015, (12) WSCAR 2016, (13) WSCAR 2017

Computer skills

Languages	**: c, c^{++}, MATLAB, Python, VERILOG & VHDL.**
Operating Systems	**: Windows 2000/XP/2007.**
Software used	**: MATLAB, Python, Xilinx ISE, Vivado, Mentor graphics, Cadence & Synopsys.**

Awards and Achievements

- Awarded for "Young Personality of the Year Award (Below 40 years)" by International Academic and Research Excellence Awards (IARE-2019).
- JSS Research Fellowship for PhD in 2014.
- GATE 2014 qualify with GATE score 357.
- "Best of best" award in 2013 at I.F.I.T, Bhopal.
- Score 98.7 percentile in MAT 2009.

Personal Vitae

Date of Birth : 28. Feb.1984

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References

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